

## N-Channel 20V(D-S) MOSFET

Product summary		
$V_{DS}$	20	V
$R_{DS(ON)}$ (at $V_{GS}=4.5V$ ) Typ.	10	$m\Omega$
$R_{DS(ON)}$ (at $V_{GS}=2.5V$ ) Typ.	12.5	$m\Omega$
$I_D(T_A=25^\circ C)$	12	A

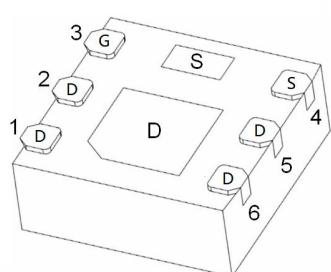
### Features

- Trench Power LV MOSFET technology
- Low  $R_{DS(ON)}$
- RoHS and Halogen-Free compliant

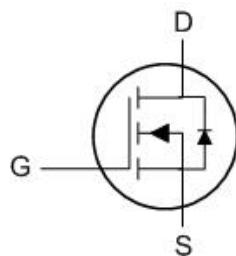
### Applications

- Load switch
- PWM application

### Pin Configuration



DFN2X2-6L



### Packing Information

Device	Package	Reel Size	Quantity(Min. Package)
ECG2012A	DFN2X2-6L	7"	3000pcs

### Absolute Maximum Ratings (at $T_A=25^\circ C$ Unless Otherwise Noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	20	V
$V_{GS}$	Gate-Source Voltage	$\pm 10$	V
$I_D$	Continuous Drain Current <sup>A</sup>	$T_C=25^\circ C$	A
		$T_C=70^\circ C$	A
$I_{DM}$	Pulse Drain Current Tested <sup>B</sup>	50	A
$P_D$	Power Dissipation <sup>C</sup>	2.5	W
$T_J, T_{STG}$	Junction and Storage Temperature Range	-55 to +150	°C

### Thermal Characteristics

Symbol	Parameter	Typical	Units
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient <sup>A</sup>	50	°C/W

Electrical Characteristics (at  $T_J = 25^\circ\text{C}$  Unless Otherwise Noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Static Parameters						
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	20	--	--	V
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{\text{DS}}=20\text{V}, V_{\text{GS}}=0\text{V}$	--	--	1	$\mu\text{A}$
$I_{\text{GSS}}$	Gate-Body Leakage Current	$V_{\text{DS}}=0\text{V}, V_{\text{GS}}=\pm 10\text{V}$	--	--	$\pm 100$	nA
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	0.45	0.6	1.0	V
$R_{\text{DS}(\text{ON})}$	Drain-Source On-State Resistance <sup>B</sup>	$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=5\text{A}$	--	10	13	$\text{m}\Omega$
		$V_{\text{GS}}=2.5\text{V}, I_{\text{D}}=3\text{A}$	--	12.5	16	$\text{m}\Omega$
		$V_{\text{GS}}=1.8\text{V}, I_{\text{D}}=2\text{A}$	--	17	25	$\text{m}\Omega$
$V_{\text{SD}}$	Diode Forward Voltage	$I_{\text{S}}=5\text{A}, V_{\text{GS}}=0\text{V}$	--	--	1.2	V
Dynamic Parameters <sup>D</sup>						
$C_{\text{iss}}$	Input Capacitance	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=10\text{V}$ $f=1\text{MHz}$	--	777	--	pF
$C_{\text{oss}}$	Output Capacitance		--	164	--	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance		--	140	--	pF
$Q_g$	Total Gate Charge	$V_{\text{DS}}=10\text{V}, I_{\text{D}}=5.6\text{A}$ $V_{\text{GS}}=4.5\text{V}$	--	25.5	--	nC
$Q_{\text{gs}}$	Gate-Source Charge		--	2.8	--	nC
$Q_{\text{gd}}$	Gate-Drain Charge		--	4.6	--	nC
$t_{\text{D}(\text{on})}$	Turn-on Delay Time	$V_{\text{DS}}=10\text{V}$ $I_{\text{D}}=1\text{A}, R_{\text{GEN}}=3\Omega$ , $V_{\text{GS}}=4.5\text{V}$	--	4.4	--	ns
$t_r$	Turn-on Rise Time		--	28.2	--	ns
$t_{\text{D}(\text{off})}$	Turn-off Delay Time		--	16.2	--	ns
$t_f$	Turn-off Fall Time		--	26	--	ns

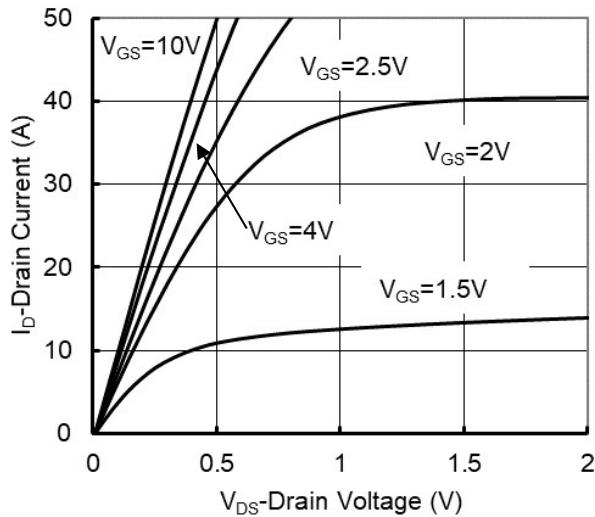
A. The data tested by surface mounted on a 1 inch x 1 inch FR-4 board with 2OZ copper.

B. Pulse Test: Pulse Width  $\leq 300\text{us}$ , Duty cycle  $\leq 2\%$ .

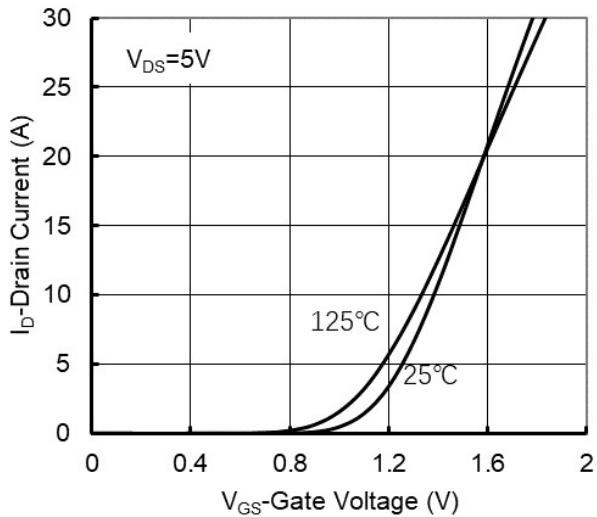
C. The power dissipation is limited by  $150^\circ\text{C}$  junction temperature.

D. Guaranteed by design, not subject to production testing.

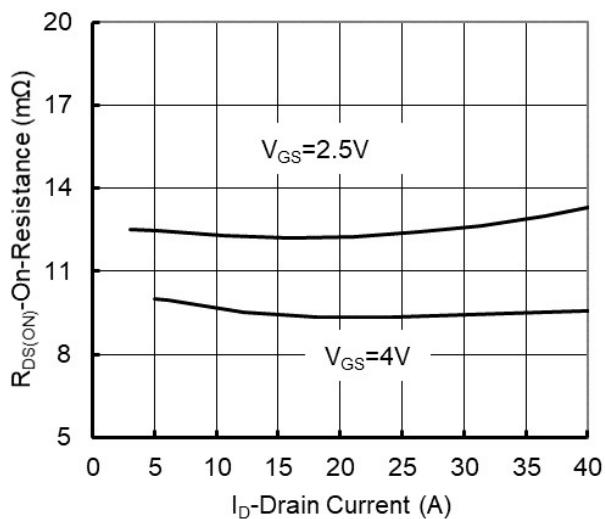
## Typical Characteristics



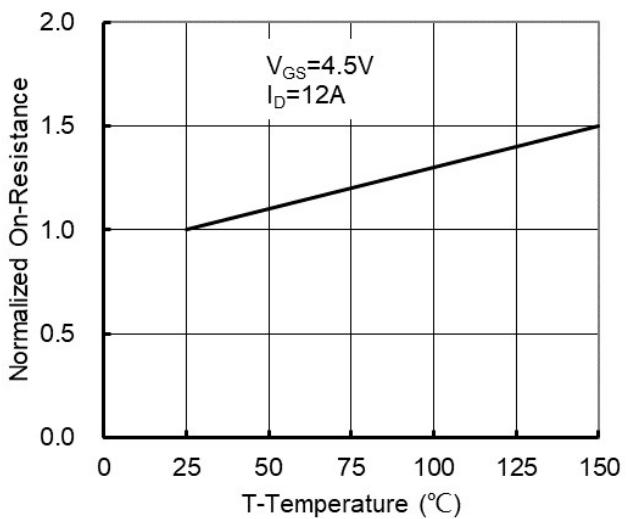
**Figure 1. Output Characteristics**



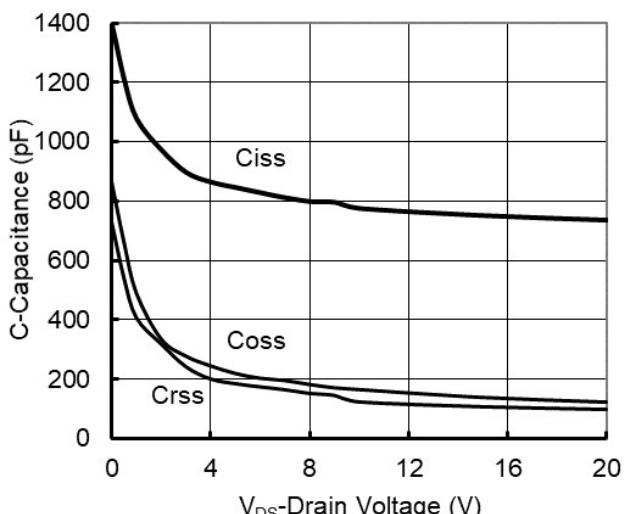
**Figure 2. Transfer Characteristics**



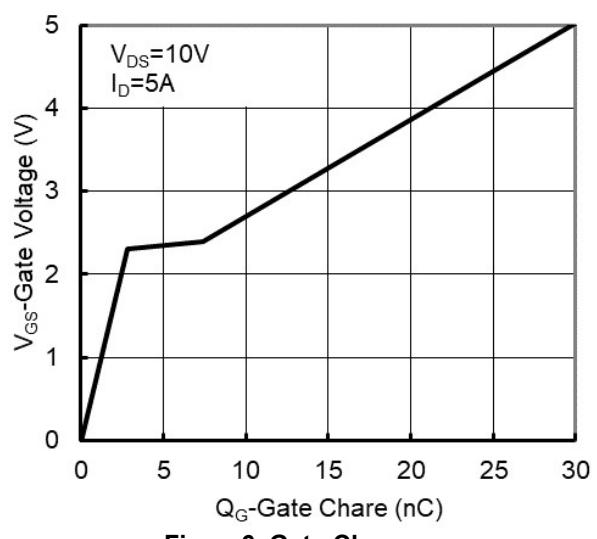
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**



**Figure 4: On-Resistance vs. Junction Temperature**

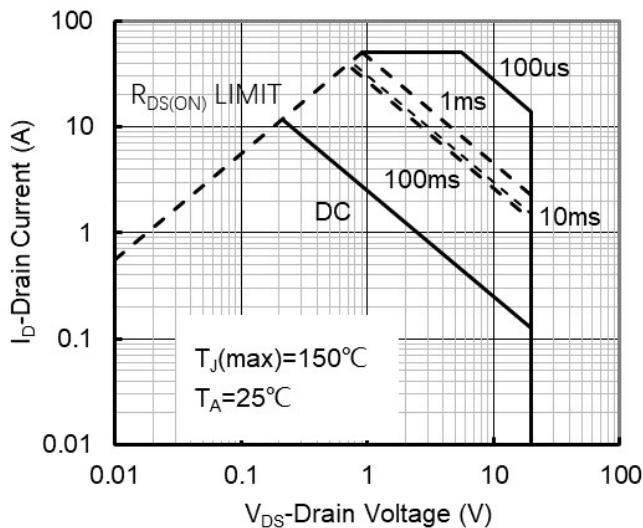


**Figure 5. Capacitance Characteristics**

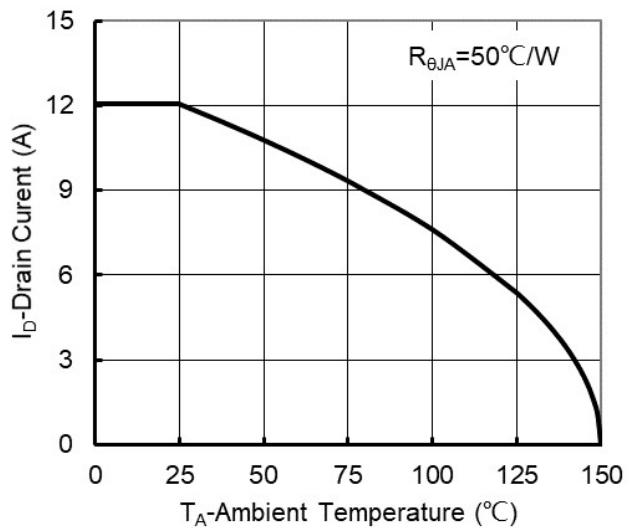


**Figure 6. Gate Charge**

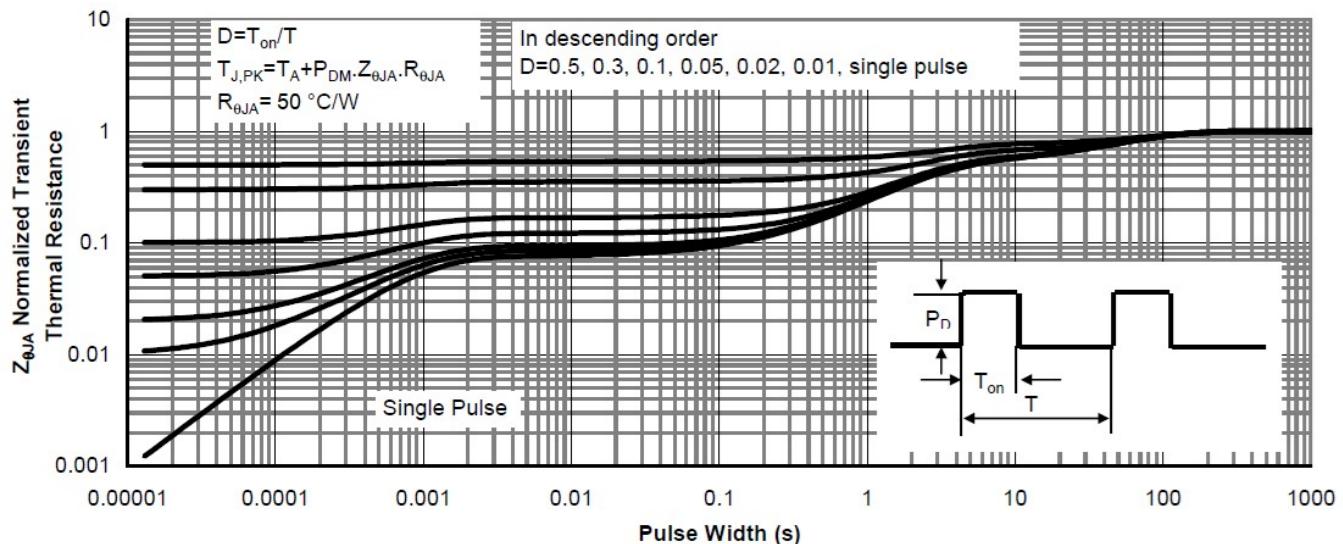
## Typical Characteristics



**Figure7. Safe Operation Area**

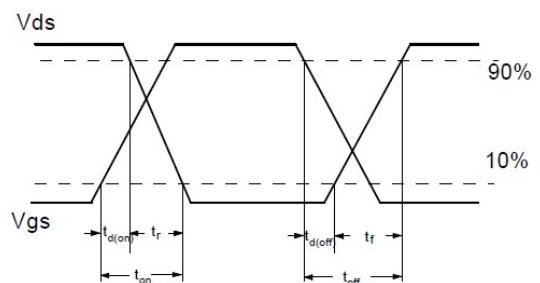
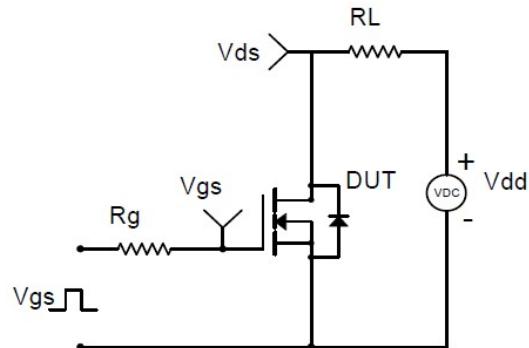


**Figure8. Maximum Continuous Drain Current vs Ambient Temperature**

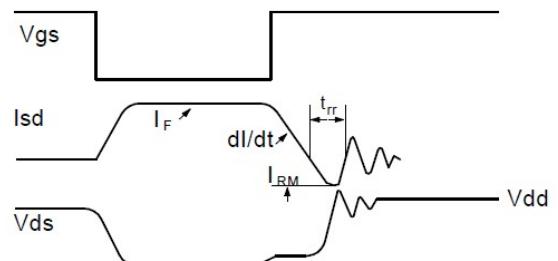
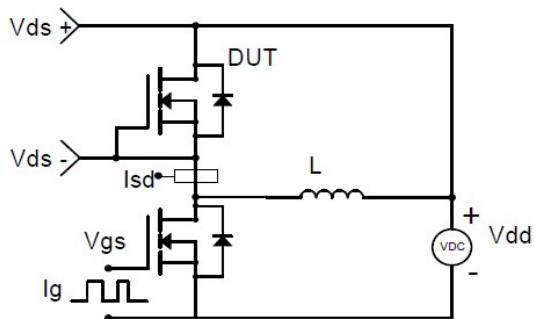


**Figure9. Normalized Maximum Transient Thermal Impedance**

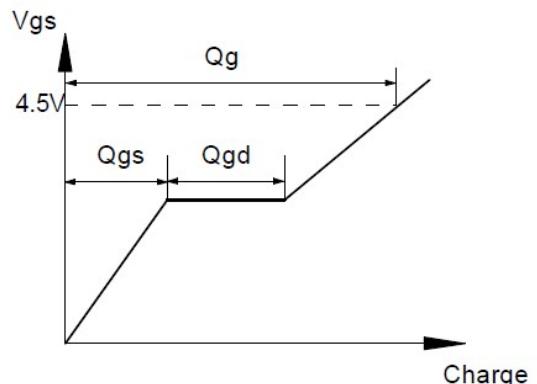
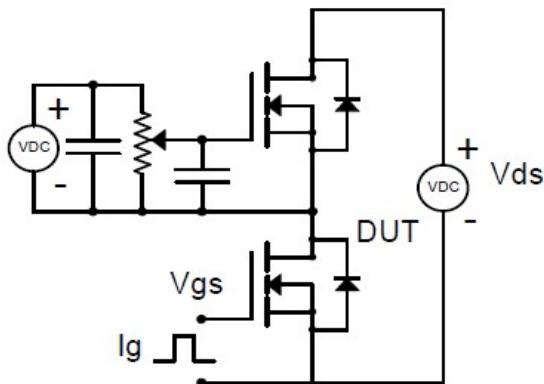
## Typical Characteristics



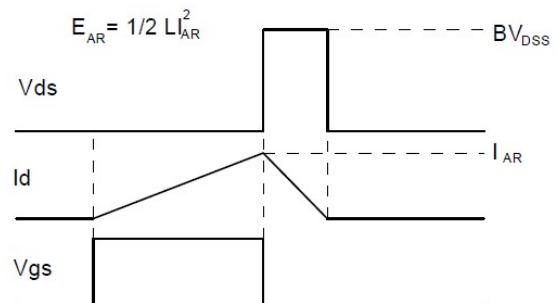
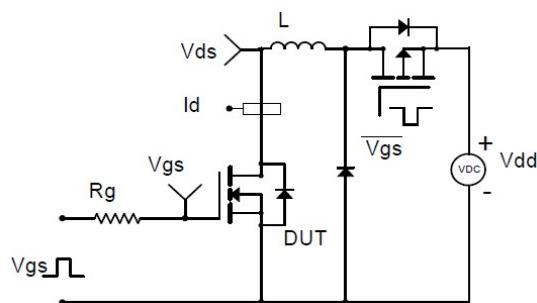
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**

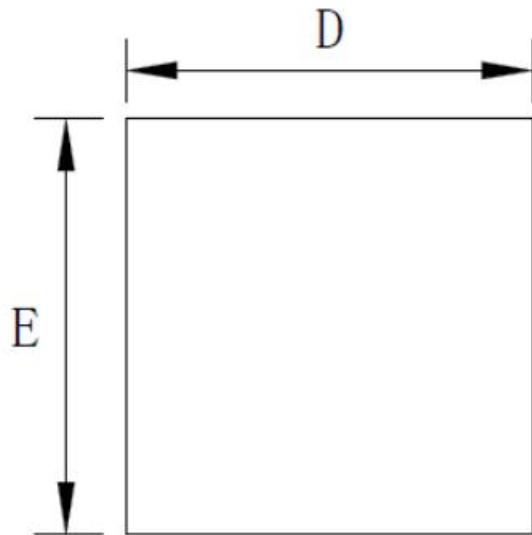


**Gate Charge Test Circuit & Waveform**

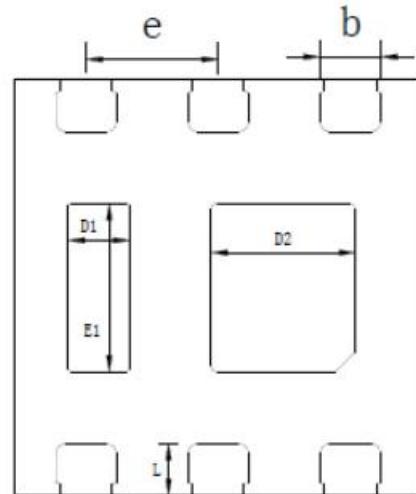


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**

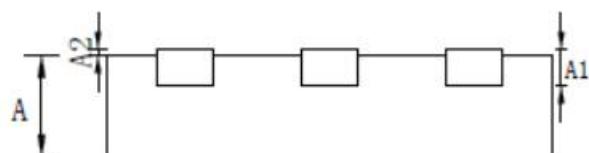
## DFN2X2-6L Package Information



Top View  
【顶视图】



Bottom View  
【背视图】



Side View  
【侧视图】

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.40	0.45	0.50
A1		0.15REF	
A2	0.00	0.02	0.05
L	0.20	0.25	0.30
b	0.25	0.30	0.35
D	1.95	2.00	2.05
E	1.95	2.00	2.05
e		0.65BSC	
D2	0.61	0.71	0.81
D1	0.20	0.30	0.40
E1	0.71	0.81	0.91