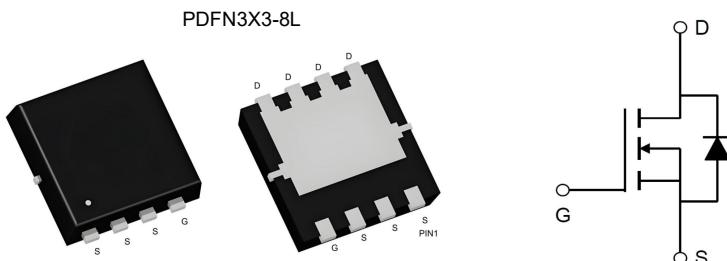


N-Channel 60V(D-S) MOSFET

Product summary			Features
V_{DS}	60	V	<ul style="list-style-type: none"> Advanced Split Gate Trench Technology Low $R_{DS(ON)}$
$R_{DS(ON)}$ (at $V_{GS}=10V$) Typ.	3.9	$m\Omega$	Applications
$R_{DS(ON)}$ (at $V_{GS}=4.5V$) Typ.	5	$m\Omega$	<ul style="list-style-type: none"> Load switching PWM Applications Power Management
$I_D(T_C=25^\circ C)$	68	A	

Pin Configuration



Packing Information

Device	Package	Reel Size	Quantity(Min. Package)
ECAL68N06	PDFN3X3-8L	13 "	5000pcs

Absolute Maximum Ratings (at $T_A=25^\circ C$ Unless Otherwise Noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current	68	A
		43	A
I_{DM}	Pulse Drain Current Tested ^A	272	A
E_{AS}	Single Pulse Avalanche Energy ^B	100	mJ
P_D	Power Dissipation $T_C=25^\circ C$	37	W
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to +150	$^\circ C$

Thermal Characteristics

Symbol	Parameter	Typical	Units
$R_{\theta JC}$	Thermal Resistance-Junction to case max	3.4	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance-Junction to ambient max ^C	27.8	$^\circ C/W$

Electrical Characteristics (at $T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Static Parameters						
BV_{DSS}	Drain-Source Breakdown Voltage	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_{\text{D}}=250\mu\text{A}$	60	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$\text{V}_{\text{DS}}=60\text{V}, \text{V}_{\text{GS}}=0\text{V}$	--	--	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$\text{V}_{\text{DS}}=0\text{V}, \text{V}_{\text{GS}}=\pm 20\text{V}$	--	--	± 100	nA
$\text{V}_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$\text{V}_{\text{DS}}=\text{V}_{\text{GS}}, \text{I}_{\text{D}}=250\mu\text{A}$	1.2	1.6	2.5	V
$\text{R}_{\text{DS}(\text{ON})}$	Drain-Source On-State Resistance ^D	$\text{V}_{\text{GS}}=10\text{V}, \text{I}_{\text{D}}=20\text{A}$	--	3.9	5.1	$\text{m}\Omega$
		$\text{V}_{\text{GS}}=4.5\text{V}, \text{I}_{\text{D}}=10\text{A}$	--	5	6.5	$\text{m}\Omega$
V_{SD}	Diode Forward Voltage	$\text{I}_{\text{S}}=20\text{A}, \text{V}_{\text{GS}}=0\text{V}$	--	--	1.2	V
Dynamic Parameters ^E						
C_{iss}	Input Capacitance	$\text{V}_{\text{GS}}=0\text{V}, \text{V}_{\text{DS}}=30\text{V}$ $f=1\text{MHz}$	--	2050	--	pF
C_{oss}	Output Capacitance		--	660	--	pF
C_{rss}	Reverse Transfer Capacitance		--	28	--	pF
Q_{g}	Total Gate Charge	$\text{V}_{\text{DS}}=30\text{V}, \text{I}_{\text{D}}=20\text{A}$ $\text{V}_{\text{GS}}=0 \text{ to } 10\text{V}$	--	35	--	nC
Q_{gs}	Gate-Source Charge		--	10	--	nC
Q_{gd}	Gate-Drain Charge		--	7	--	nC
$t_{\text{D}(\text{on})}$	Turn-on Delay Time	$\text{V}_{\text{DD}}=30\text{V}$ $, \text{R}_{\text{GEN}}=4.5\Omega,$ $\text{I}_{\text{D}}=20\text{A},$ $\text{V}_{\text{GS}}=10\text{V}$	--	12	--	ns
t_{r}	Turn-on Rise Time		--	34	--	ns
$t_{\text{D}(\text{off})}$	Turn-off Delay Time		--	25	--	ns
t_{f}	Turn-off Fall Time		--	30	--	ns
t_{rr}	Reverse recovery time	$\text{I}_{\text{F}}=20\text{A},$ $d\text{i}/dt=100\text{A}/\mu\text{s}$	--	38	--	ns
Q_{rr}	Reverse recovery charge		--	23	--	nC

A. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.

B. EAS condition: $T_J=25^\circ\text{C}$, $\text{V}_{\text{DD}}=30\text{V}$, $\text{R}_G=25\Omega$, $\text{V}_{\text{G}}=10\text{V}$, $\text{L}=0.5\text{mH}$, $\text{I}_{\text{AS}}=20\text{A}$.

C. The data tested by surface mounted on a 1 inch x 1 inch FR-4 board with 2OZ copper.

D. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.

E. Guaranteed by design, not subject to production testing.

Typical Characteristics

Figure 1: Output Characteristics

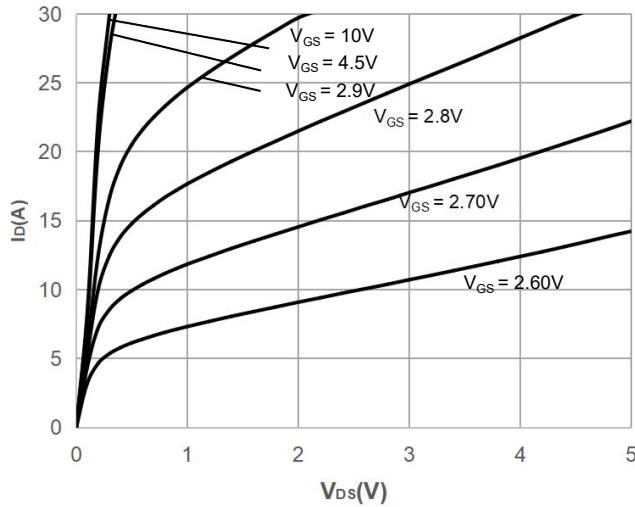


Figure 2: Typical Transfer Characteristics

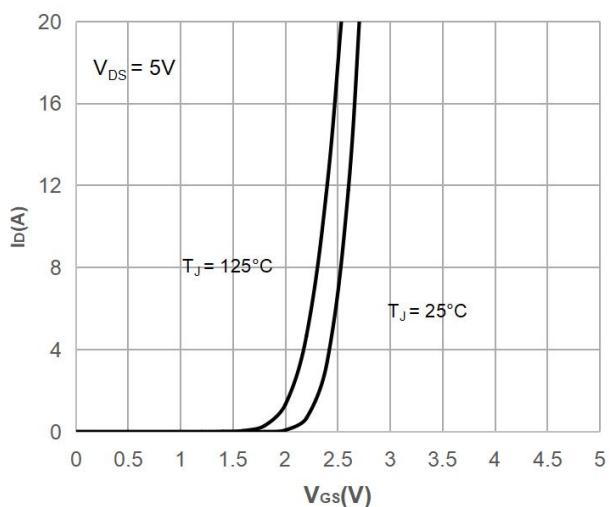


Figure 3: On-resistance vs. Drain Current

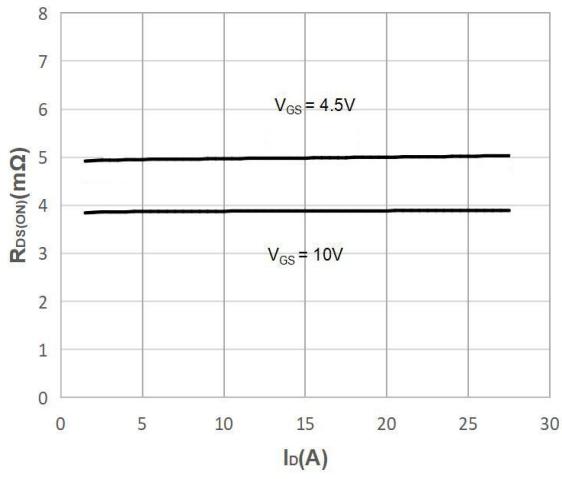


Figure 4: Body Diode Characteristics

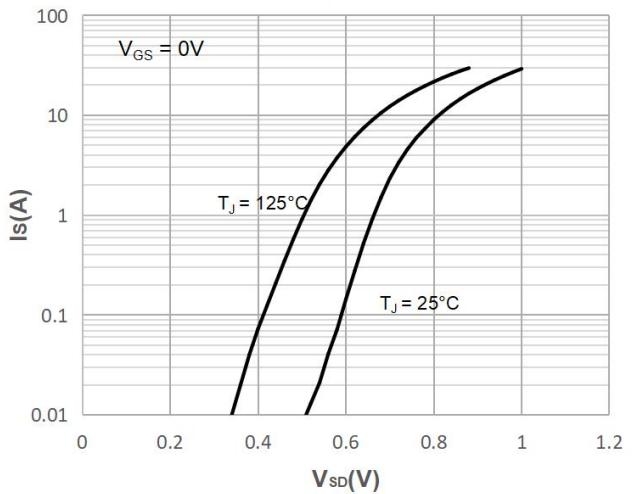


Figure 5: Gate Charge Characteristics

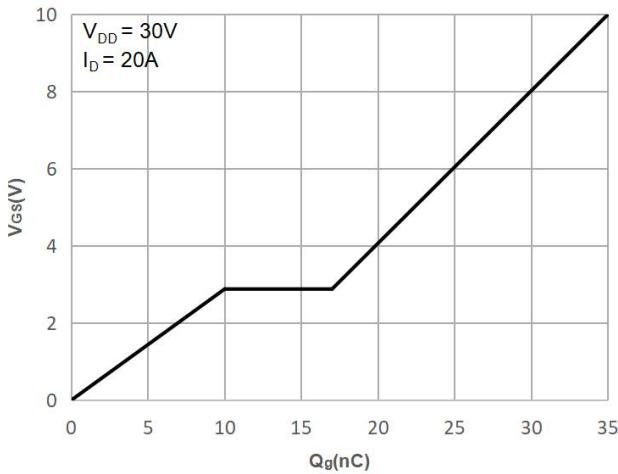
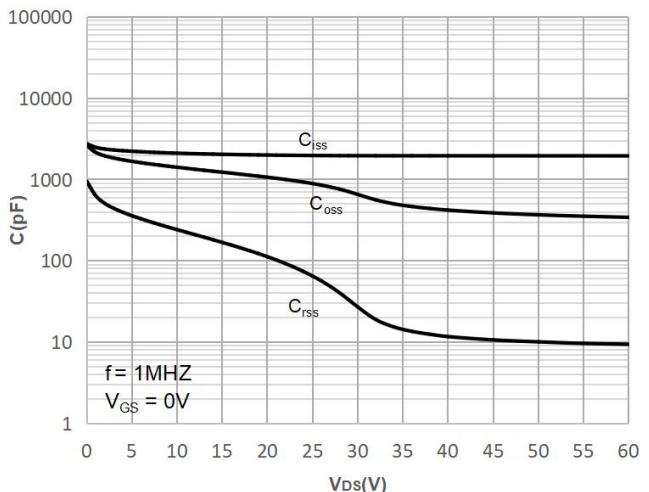


Figure 6: Capacitance Characteristics



Typical Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

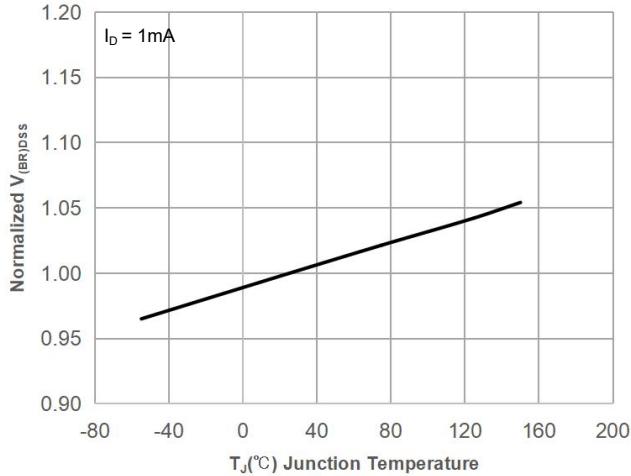


Figure 8: Normalized on Resistance vs. Junction Temperature

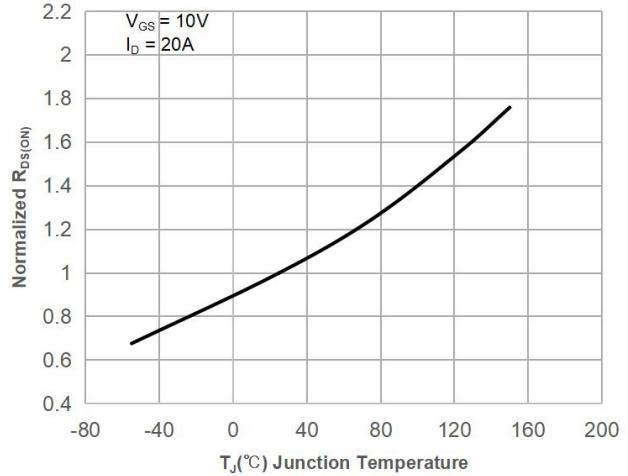


Figure 9: Maximum Safe Operating Area

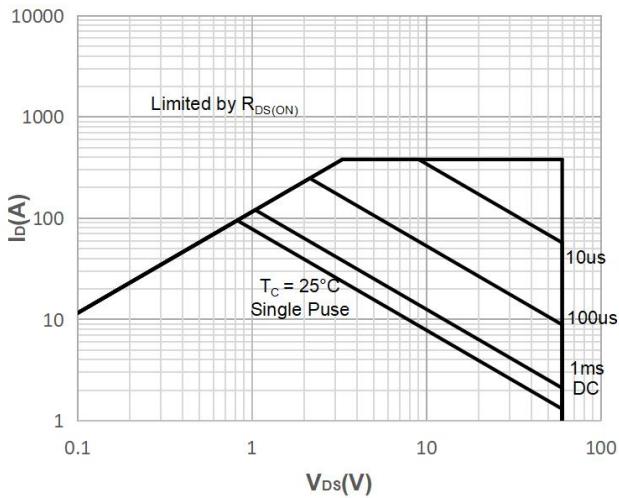


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

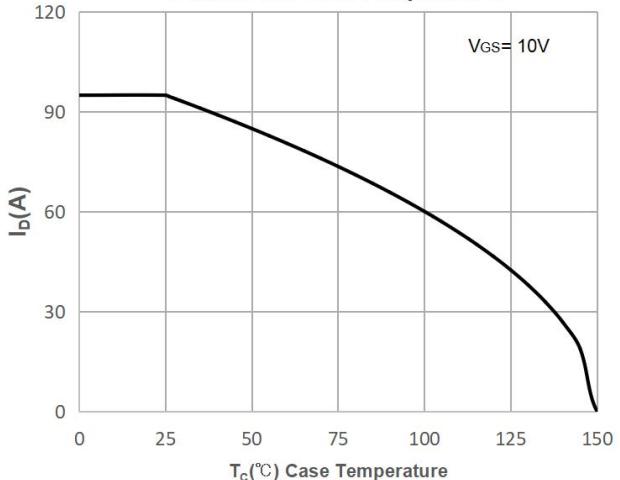


Figure 11: Normalized Maximum Transient Thermal Impedance

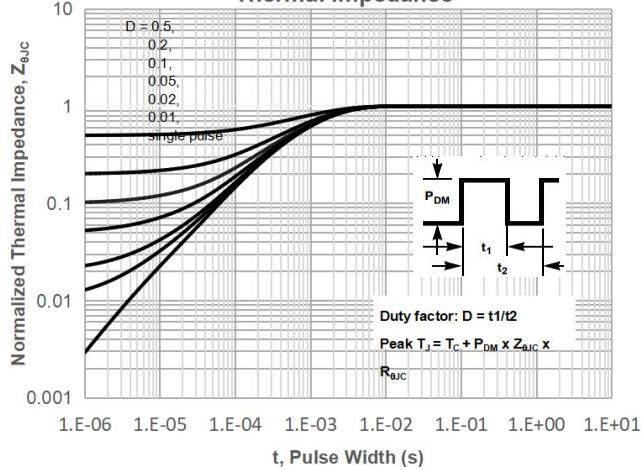
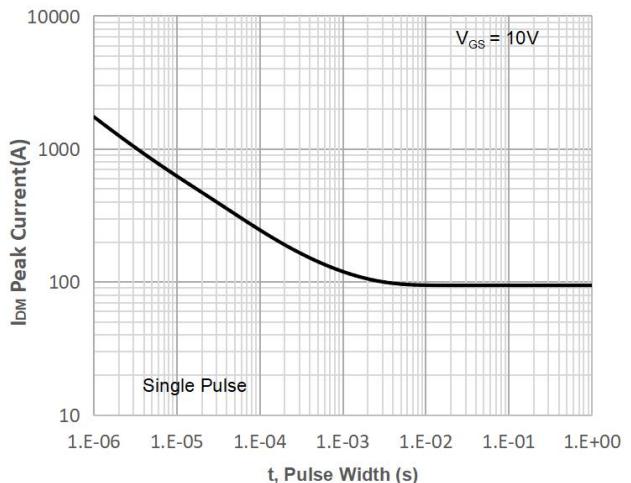


Figure 12: Peak Current Capacity



Test Circuit

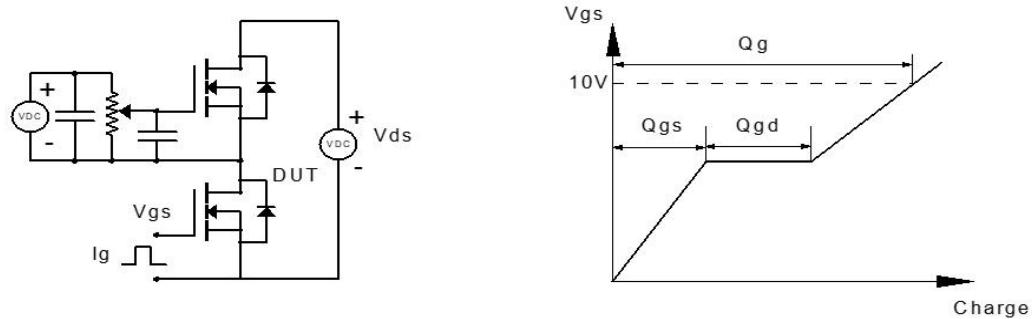


Figure 1: Gate Charge Test Circuit & Waveform

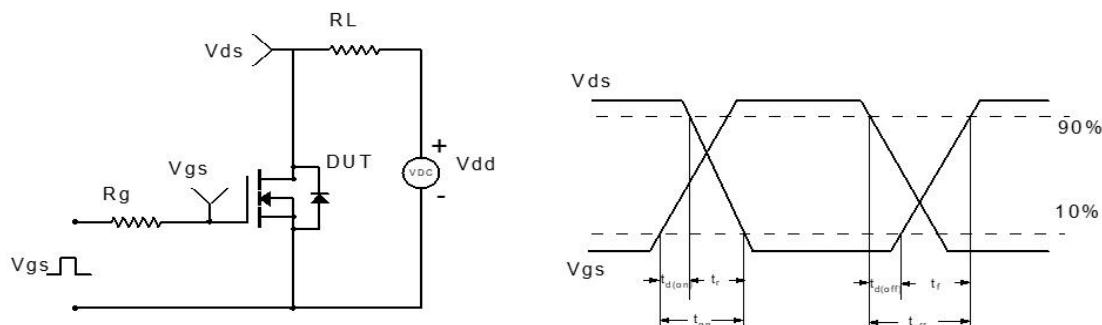


Figure 2: Resistive Switching Test Circuit & Waveform

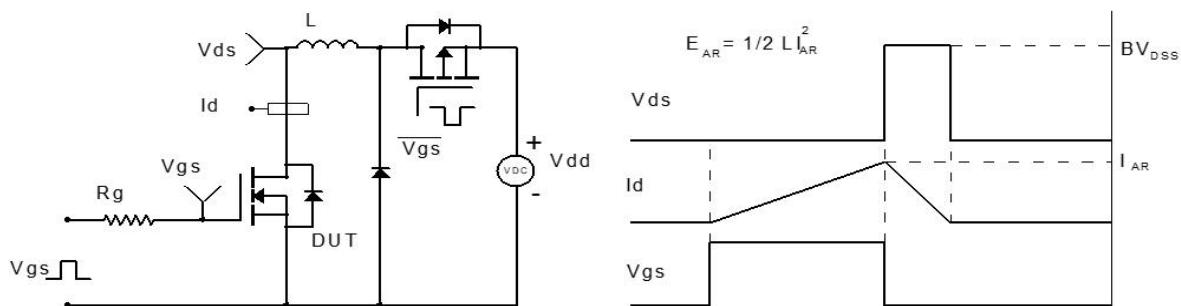


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

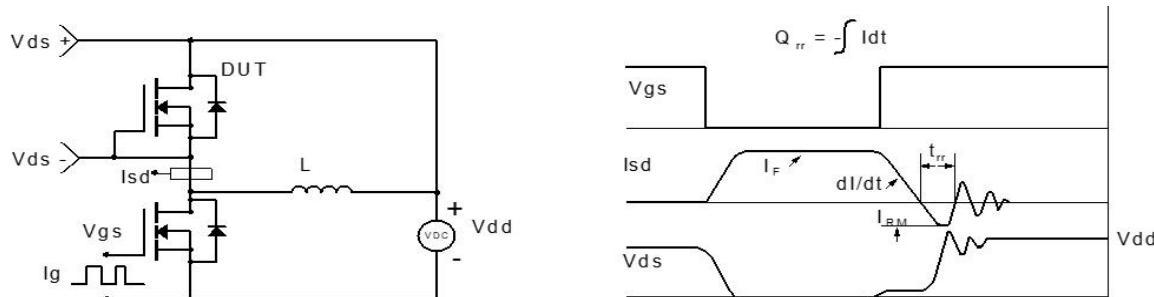
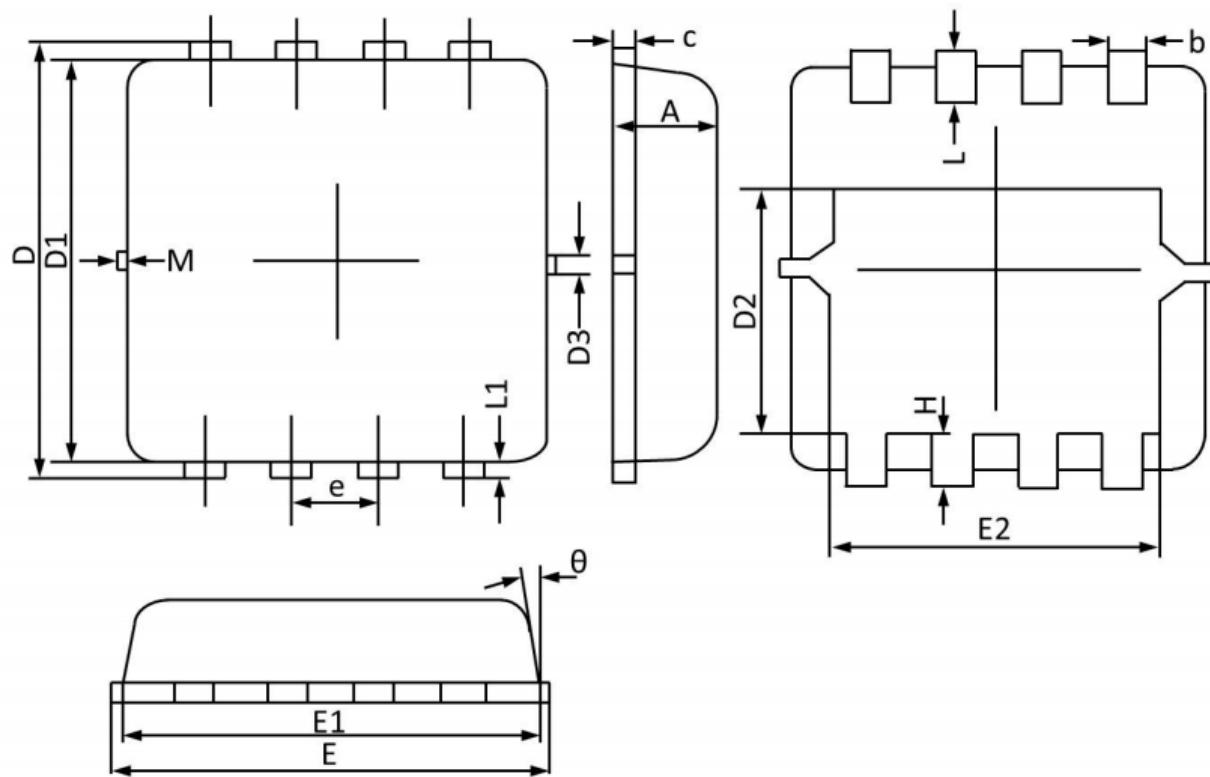


Figure 4: Diode Recovery Test Circuit & Waveform

PDFN3X3-8L Package Information (unit:mm)


DIMENSIONS

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	0.70	0.75	0.80	b	0.25	0.30	0.35
C	0.10	0.15	0.25	D	3.25	3.35	3.45
D1	3.00	3.10	3.20	D2	1.78	1.88	1.98
D3	--	0.13	--	E	3.20	3.30	3.40
E1	3.00	3.15	3.20	E2	2.39	2.49	2.59
e	0.65BSC			H	0.30	0.39	0.50
L	0.30	0.40	0.50	L1	--	0.13	--
θ	--	10°	12°	M	*	*	0.15