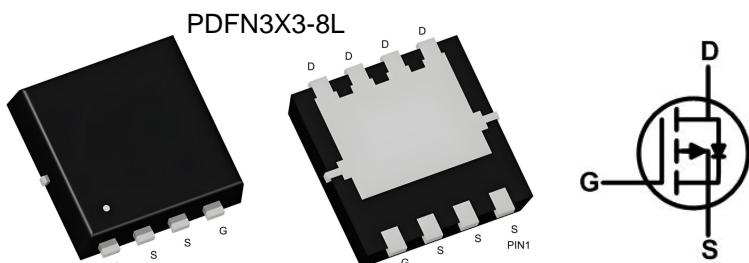


P-Channel 30V(D-S) MOSFET

Product summary			Features		
V_{DS}	-30	V	• Advanced Trench technology		
$R_{DS(ON)}$ (at $V_{GS}=-10V$) Typ.	8	$m\Omega$	• Low Gate Charge		
$R_{DS(ON)}$ (at $V_{GS}=-4.5V$) Typ.	11	$m\Omega$	Applications		
$I_D(T_c=25^\circ C)$	-42	A	• Load switching		

Pin Configuration



Packing Information

Device	Package	Reel Size	Quantity(Min. Package)
ECAL42P03	PDFN3X3-8L	13"	5000pcs

Absolute Maximum Ratings (at $T_A=25^\circ C$ Unless Otherwise Noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current	-42	A
		-26.6	A
I_{DM}	Pulse Drain Current Tested ^A	-166	A
E_{AS}	Single Pulse Avalanche Energy ^B	45	mJ
P_D	Power Dissipation $T_c=25^\circ C$	37	W
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to +150	$^\circ C$

Thermal Characteristics

Symbol	Parameter	Typical	Units
$R_{\theta JA}$	Thermal Resistance-Junction to ambient max ^C	75	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance-Junction to case max	3.4	$^\circ C/W$

Electrical Characteristics (at $T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Static Parameters						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=-250\mu\text{A}$	-30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}}=-30\text{V}, V_{\text{GS}}=0\text{V}$	--	--	-1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{\text{DS}}=0\text{V}, V_{\text{GS}}=\pm 20\text{V}$	--	--	± 100	nA
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=-250\mu\text{A}$	-1.0	-1.9	-2.5	V
$R_{\text{DS}(\text{ON})}$	Drain-Source On-State Resistance ^D	$V_{\text{GS}}=-10\text{V}, I_{\text{D}}=-30\text{A}$	--	8	10	$\text{m}\Omega$
		$V_{\text{GS}}=-4.5\text{V}, I_{\text{D}}=-15\text{A}$	--	11	14	$\text{m}\Omega$
V_{SD}	Diode Forward Voltage	$I_{\text{S}}=-1\text{A}, V_{\text{GS}}=0\text{V}$	--	--	-1.2	V
Dynamic Parameters ^E						
C_{iss}	Input Capacitance	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=-15\text{V}$ $f=1\text{MHz}$	--	2360	--	pF
C_{oss}	Output Capacitance		--	325	--	pF
C_{rss}	Reverse Transfer Capacitance		--	281	--	pF
Q_g	Total Gate Charge	$V_{\text{DS}}=-15\text{V}, I_{\text{D}}=-30\text{A}$ $V_{\text{GS}}=-10\text{V}$	--	30	--	nC
Q_{gs}	Gate-Source Charge		--	5	--	nC
Q_{gd}	Gate-Drain Charge		--	7.5	--	nC
$t_{\text{D}(\text{on})}$	Turn-on Delay Time	$V_{\text{DS}}=-15\text{V}$ $I_{\text{D}}=-30\text{A}, V_{\text{GS}}=-10\text{V},$ $R_{\text{GEN}}=3\Omega$	--	14	--	ns
t_r	Turn-on Rise Time		--	20	--	ns
$t_{\text{D}(\text{off})}$	Turn-off Delay Time		--	94	--	ns
t_f	Turn-off Fall Time		--	65	--	ns
t_{rr}	Reverse recovery time	$I_{\text{F}}=-30\text{A},$ $di/dt=-100 \text{ A}/\mu\text{s}$	--	19	--	ns
Q_{rr}	Reverse recovery charge		--	9	--	nC

Note:

- A. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
- B. The EAS data shows Max. rating . The test condition is $V_{\text{DD}}=-25\text{V}, V_{\text{G}}=-10\text{V}, L=0.1\text{mH}, I_{\text{AS}}=-30\text{A}, R_{\text{g}}=25\Omega, T_J=25^\circ\text{C}$.
- C. The data tested by surface mounted on a 1 inch x 1 inch FR-4 board with 2OZ copper.
- D. Pulse Test: Pulse Width $\leq 300\text{us}$, Duty cycle $\leq 2\%$.
- E. Guaranteed by design, not subject to production testing.

Typical Characteristics

Figure 1: Output Characteristics

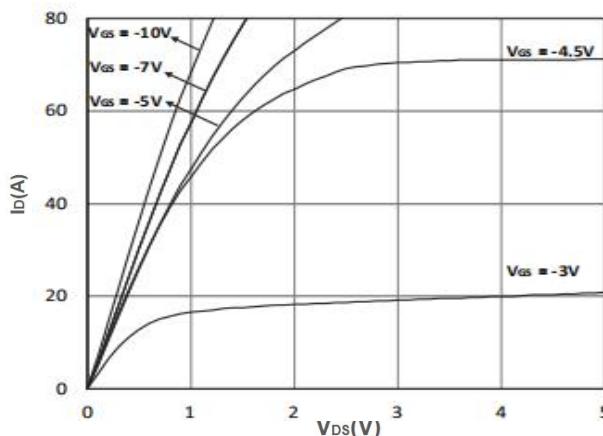


Figure 2: Typical Transfer Characteristics

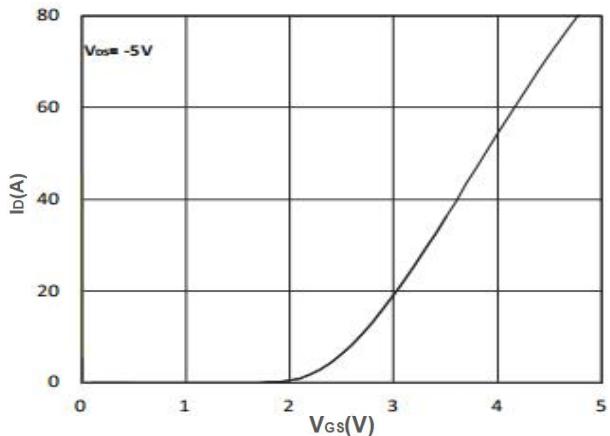


Figure 3: On-resistance vs. Drain Current

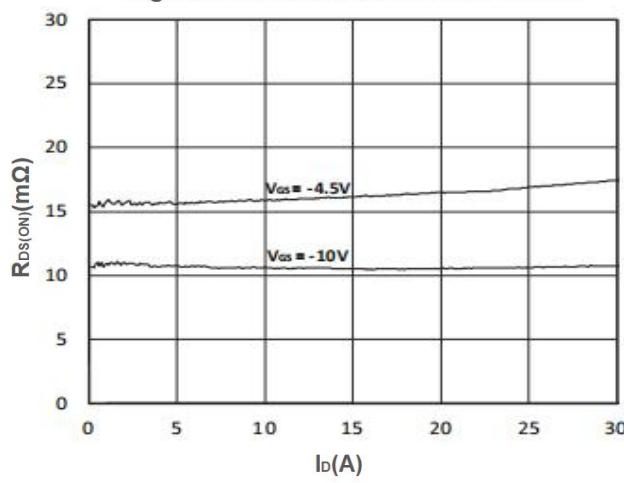


Figure 4: Body Diode Characteristics

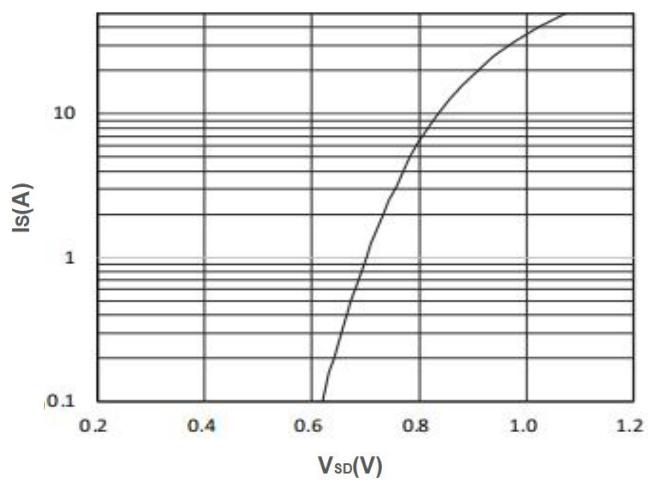


Figure 5: Gate Charge Characteristics

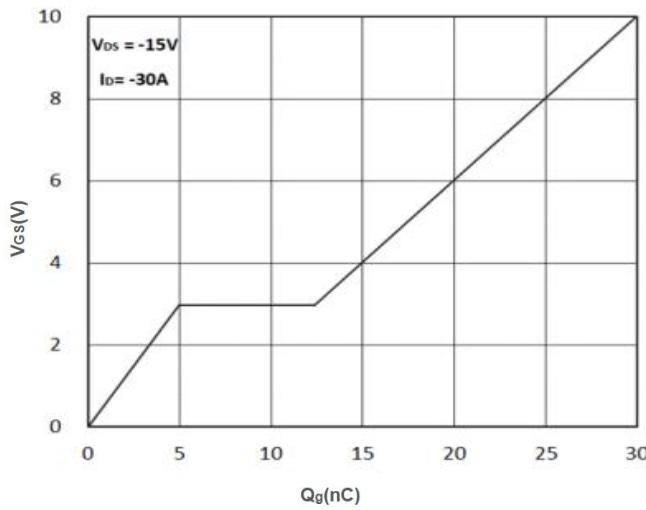
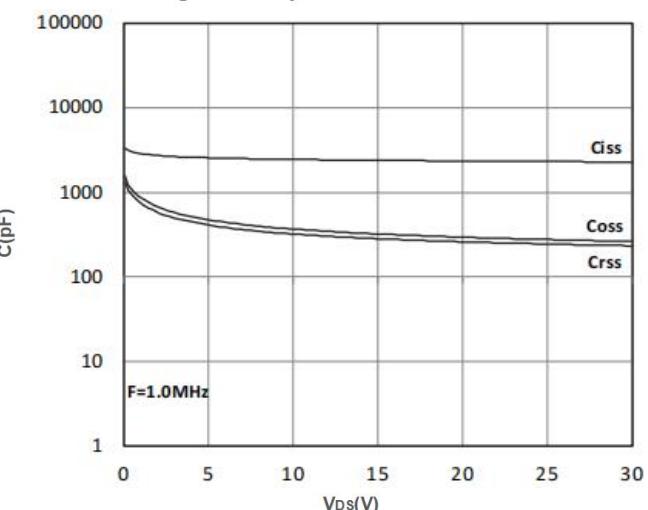


Figure 6: Capacitance Characteristics



Typical Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

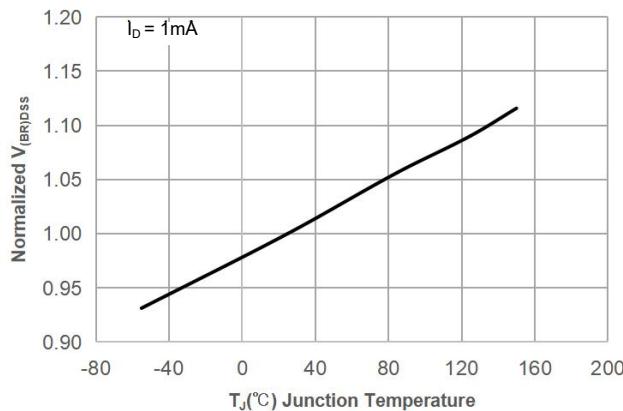


Figure 8: Normalized on Resistance vs. Junction Temperature

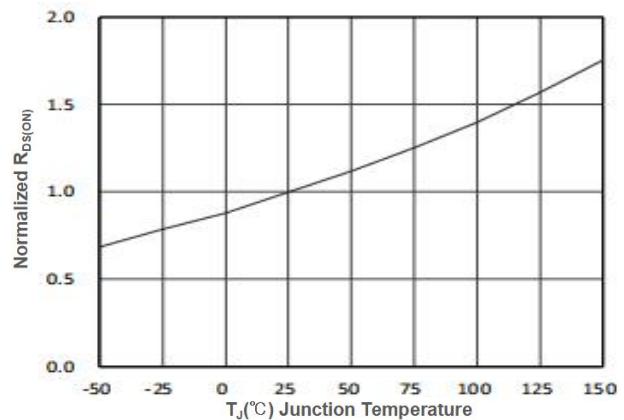


Figure 9: Maximum Safe Operating Area

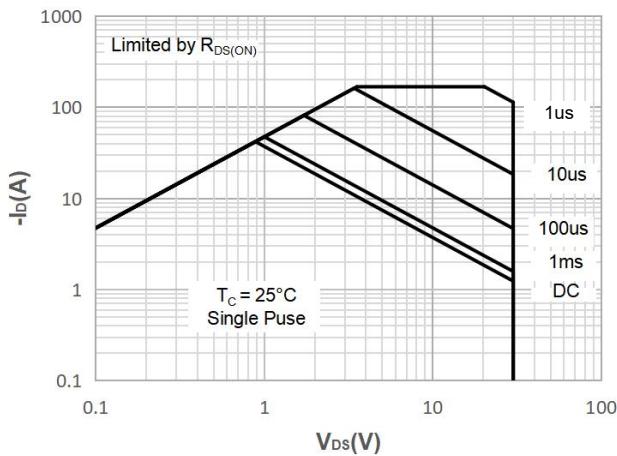


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

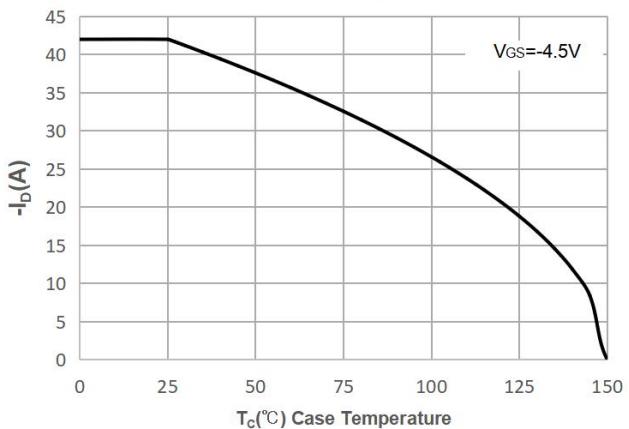


Figure 11: Normalized Maximum Transient Thermal Impedance

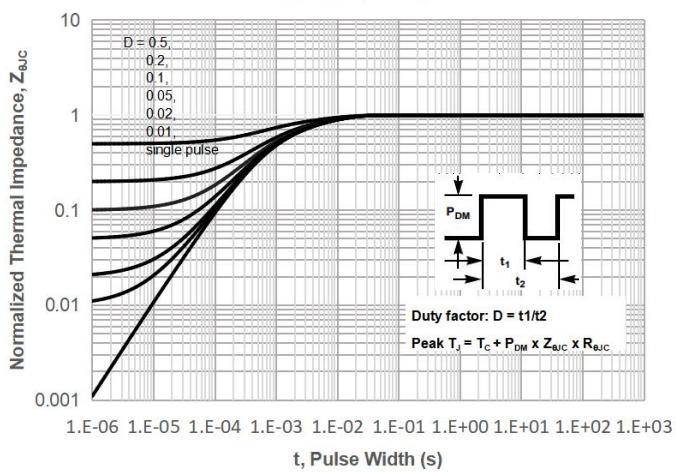
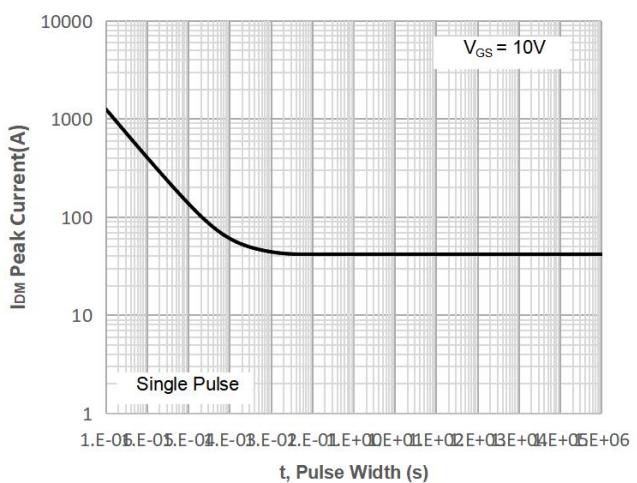


Figure 12: Peak Current Capacity



Test Circuit

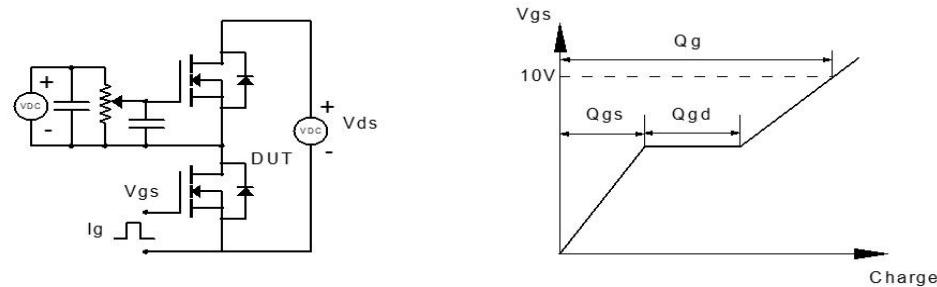


Figure 1: Gate Charge Test Circuit & Waveform

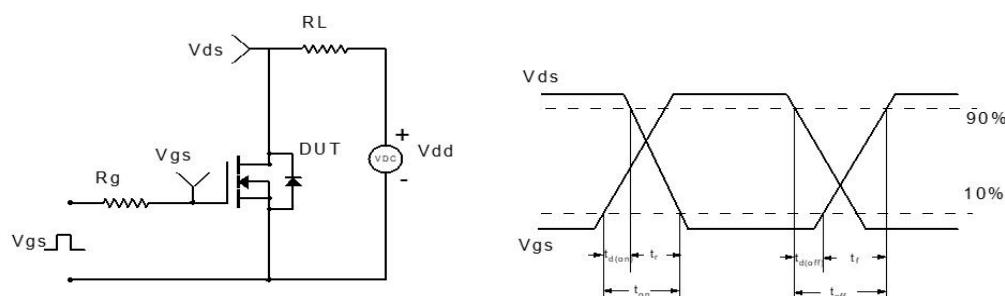


Figure 2: Resistive Switching Test Circuit & Waveform

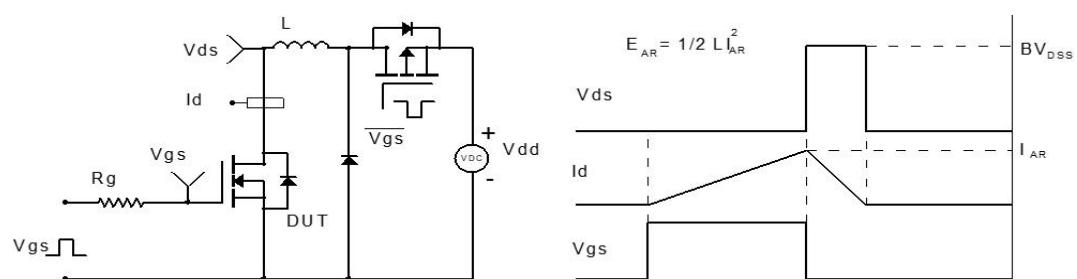


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

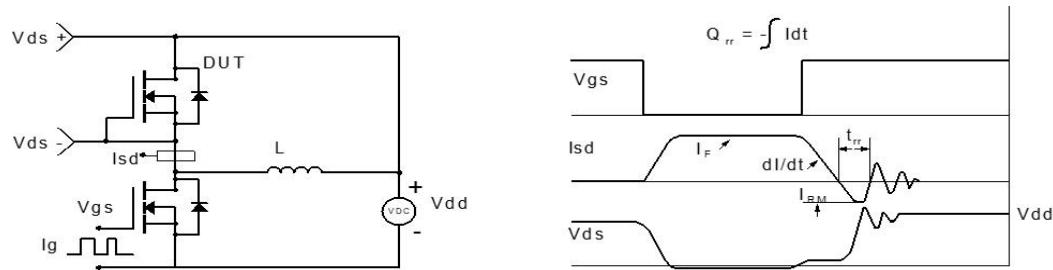
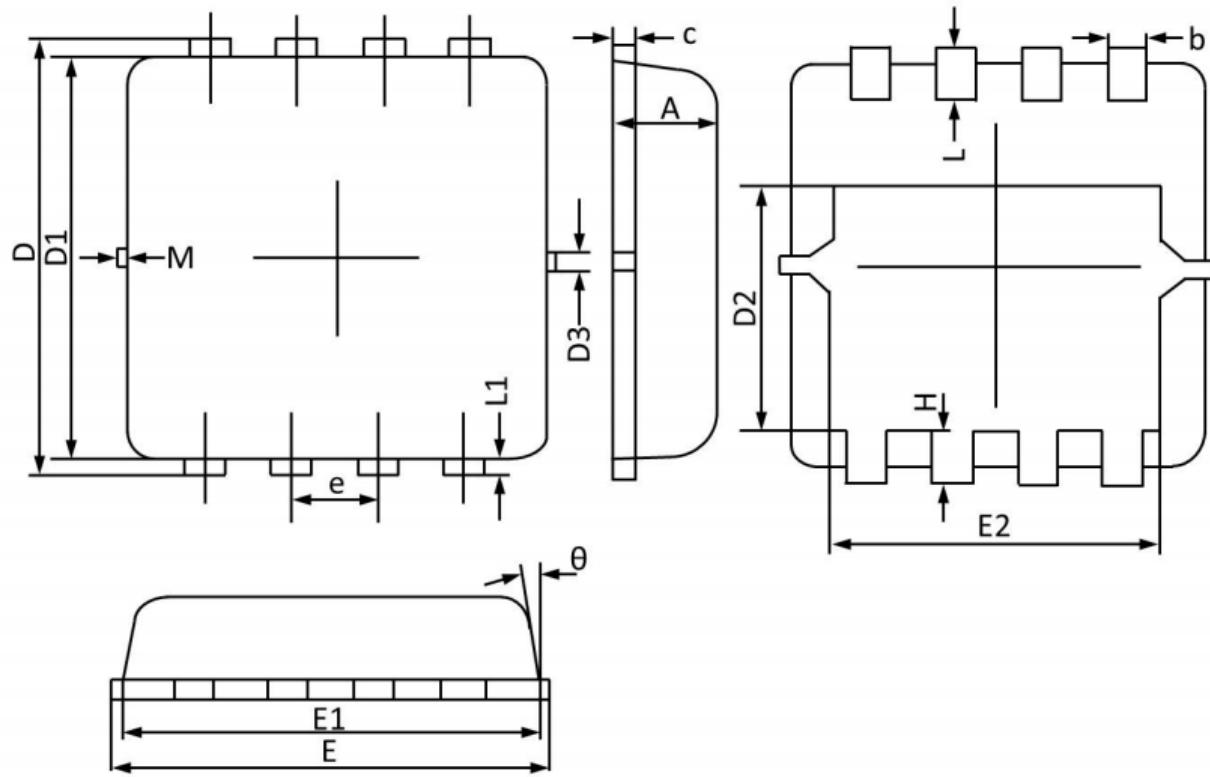


Figure 4: Diode Recovery Test Circuit & Waveform

PDFN3X3-8L Package Information (unit:mm)


DIMENSIONS

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	0.70	0.75	0.80	b	0.25	0.30	0.35
C	0.10	0.15	0.25	D	3.25	3.35	3.45
D1	3.00	3.10	3.20	D2	1.78	1.88	1.98
D3	--	0.13	--	E	3.20	3.30	3.40
E1	3.00	3.15	3.20	E2	2.39	2.49	2.59
e	0.65BSC			H	0.30	0.39	0.50
L	0.30	0.40	0.50	L1	--	0.13	--
θ	--	10°	12°	M	*	*	0.15